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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): MM6

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on ______

Signature ______

Typed or printed name ______

Application Number	Filed
10/804,777	3/18/04

First Named Inventor: Ichitsubo

Art Unit	Examiner
2822	Lewis

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 37,955
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 ______

Signature: [signature]

Typed or printed name: Bao Tran

Telephone number: 408 528 7490

Date: 2-18-07

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of ______ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Lewis, Monica
Ichitsubo	Art Unit: 2822
Application No.: 10/804,737	
Filed: 3/18/2004	
	PRE-APPEAL BRIEF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit this Pre-Appeal Brief, along with a Declaration in support thereof in response to the Final Office Action mailed 11/20/2006. The Final Office Action rejected claims 1-9, 11, 14 and 19-20 under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 6,642,617 (Kawai) in view of Riches and Wang. Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, Wang and Lin. Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, Wang, and *Electronic Packaging and Interconnection Handbook* by Charles A. Harper (Harper). Claims 12 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, Wang, *Microchip Fabrication* by Peter Van Zant (van Zant). Claims 15 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, Pohjonen (U.S. Patent No. 6,462,950). Claim 17 was rejected under 35 U.S.C. 103 (a) as being unpatentable over Kawai in view of Riches, Wang, Pohjonen and Van Zant. Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, Wang, Apel (U.S. Patent No. 6,727,761).

In view of the reasons set forth below, Applicants submit that all claims are in condition for allowance and respectfully submit allowance of all claims.

The Section 103 Rejection

In regards to claim 1, the Office Action asserts that Kawai discloses the following:

a) one or more active substrates (12a) comprising substantially transistors or diodes (10) formed thereon (For Example: See Figure 3 and Column 5 Lines 45 and 46);

b) one or more passive substrates (2a) comprising substantially inductors, capacitors or resistors (4) formed thereon (For Example: See Figure 3 and Column 4 Lines 17-20);

c) a plurality of bonding pads (15a and 5b) positioned on the active and passive substrates (For Example: See Figure 1);

d) bonding wires (6) connected to the bonding pads (For Example: See Figure 1).

The Office Action asserts that:

However, Riches discloses a semiconductor device that has a plurality of active substrates (For Example: See Page 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a plurality of active substrates as disclosed in Riches because it aids in providing a support for the interconnection of various components (For Example: See Page 1).

Additionally, since Kawai and Riches are both from the same field of endeavor, the purpose disclosed by Smiths would have been recognized in the pertinent art of Riches.

b) intra-substrate pads adapted to support wire-bonding within a substrate.

However, Wang et al. ("Wang") discloses a semiconductor device that has intra-substrate pads adapted to support wire-bonding within a substrate (For Example: See Figure 2c). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include intra-substrate pads adapted to support wire-bonding within a substrate as disclosed in Wang because it aids in providing interconnection to other components (For Example: See Figure 2).

Additionally, since Kawai and Wang are both from the same field of endeavor, the purpose disclosed by Wang would have been recognized in the pertinent art of Kawai.

Applicants respectfully traverse the rejection. Kawai relates to a semiconductor device with a SAW device chip provided on a passive element chip in which a passive element circuit including a transmission line is formed on a semi-insulating compound substrate having one surface set to have a ground potential electrode.

Wang relates to a flip-chip assembly with reflowable underfill. As the Wang title suggests, Wang relates to soldering reliability. Fig. 2C in Wang shows a pad definition for soldering purposes. However, Wang's flip chip assembly does not need wire-bonding and therefore Wang fails to show the intra-substrate pads that allow wire bonding to be done within a substrate.

As noted in paragraph 4 of the attached declaration, the Wang substrate is a multi-layer material built up as the module base to attach semiconductor ICs, and is NOT a semiconductor IC itself. Wang's Fig. 2c refers to pad definitions on the module base. These pads on Fig. 2c provide bonding on the same multi-layer material that forms the supporting base, NOT the intra-substrate bonding on the IC such as the intra-substrate bondings on the IC 20 of FIG. 1 of the instant application.

Further, as noted in paragraph 5 of the attached declaration, in the instant application, the intra-substrate pads and the wire-bonding among intra-substrate pads within a semiconductor IC such as the IC 20 are done to provide electromagnetic characteristics that are useful in certain radio frequency (RF) circuitry. For example, such intra-substrate wire-bonds can be used to vary resistance/capacitance/ inductance (RCL) characteristics useful for RF circuitry. Hence, the intra-substrate bonding on the IC is

done to achieve a technical function that is different from the wiring for interconnection purposes of Kawai, Riches and Wang as asserted in the Final Office Action.

Neither Kawai, Riches, nor Wang shows as a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate. As shown in FIG. 1 of the instant application, each substrate 20, 30 and 40 may have **intra-substrate pads that allow wire-bonding to be done within a substrate**.

Moreover, the combination of Kawai, Riches, and Wang would result in an inoperable device. As stated in paragraph 6 of the declaraion, the combination of Kawai, Riches, and Wang would result in an inoperable device. Riches disclose CMOS MCM substrates. Wang discloses flip chip assembly via reflowable underfill. However, Wang's flip chip assembly technique would not work with IC dies having rough surface morphology such as the GaAs HBT IC that is used as the active die 20 in FIG. 1 of the instant application. One skilled in the art would not combine the dies of Kawai and Riches with the Wang flip-chips because such a combination would not work.

Additionally, as noted in paragraph 7 of the declaration, one skilled in the art would not have combined Kawaii, Riches and Wang to arrive at active and passive IC modules with intra-substrate pads adapted to support wire-bonding within an IC substrate. As noted at http://www.microbonding.com/gb/fc_gb.htm, "flip chip technology is cheaper than wire bonding (true also with TAB) because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time." In this case, one skilled in the art would not have done flip-chip and then wirebond two pads that are completely within an integrated circuit (IC) die. Combining the references as suggested by the Examiner would not be economical and one skilled in the art would not be motivated to combine as suggested as it is cheaper to provide interconnection using lines fabricated directly on the IC rather than to bond wires between pads on the IC.

The combination of CMOS and GaAs circuits would not provide performance WiFi circuits such as power amplifiers. Further, there is no motivation to combine Wang's soldering art with wirebonding of GaAs substrates. Hence, one skilled in the art would not combine Kawai with Riches or Wang.

Applicant notes that the present rejection does not establish *prima facie* obviousness under 35 U.S.C. § 103 and M.P.E.P. §§ 2142-2143. The Examiner bears the initial burden to establish and support *prima facie* obviousness. *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976). To establish *prima facie* obviousness, three basic criteria must be met. M.P.E.P. § 2142. First, the Examiner must show some suggestion or motivation, either in the Kawai reference or in the knowledge generally available to one of ordinary skill in the art, to modify the reference so as to produce the claimed invention. M.P.E.P. § 2143.01; *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Secondly, the Examiner must establish that there is a reasonable expectation of success for the modification. M.P.E.P. § 2142. Thirdly, the Examiner

must establish that the prior art references teach or suggest all the claim limitations. M.P.E.P. §2143.03; *In re Royka*, 180 U.S.P.Q. 580 (CCPA 1974). The teachings, suggestions, and reasonable expectations of success must be found in the prior art, rather than in Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q.2d 1438 (CAFC 1991). Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on at least two of the above requirements.

Under *Vaeck*, absent any evidence of a cited suggestion or reasonable motivation in the Norand reference, or knowledge of those skilled in the art, *prima facie* obviousness of the independent claims (and those dependent therefrom) has not been established. As such, it is respectfully requested that the § 103(a) rejection of all claims be withdrawn and the claims be allowed.

Moreover, Kawai cannot render obvious any of the dependent claims that depend from allowable claim 1. First, as discussed above, the claims are allowable as none of the references show a device with a plurality of active substrates comprising substantially transistors or diodes formed thereon; one or more passive substrates comprising substantially inductors, capacitors or resistors formed thereon; a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate; and bonding wires connected to the bonding pads. Additionally, the references do not show the structures recited in the dependent claims. As the references fail to show a number of elements of the dependent claims, withdrawal of the Section 103 rejection on these claims is requested.

CONCLUSION

Applicants submit that all claims are in condition for allowance.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the undersigned at (408) 528-7490.

Respectfully submitted,

Bao Tran

Reg. No. 37,955

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Lewis, Monica
Ichitsubo	Art Unit: 2822
Application No.: 10/804,737	**DECLARATION OF WEIPING WANG**
Filed: 3/18/2004	

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

I, Weiping Wang, declare as follows, under the penalty of perjury.

I am currently the Managing Director of Micro Mobio, Inc., the assignee of the instant application. I have over six years of experience in the wireless technology.

1. I have reviewed the Final Office Action mailed November 20, 2006 for the above referenced case. I have also reviewed USPN 6,642,617 (Kawai), Active Substrates (Riches) and Assessment of Flip Chip Assembly and Reliability via Reflowable Underfill (Wang) references used to reject claims 1-9, 11, 14, 19 and 20.

2. I noted the following statement from the Final Office Action relating to the claimed intra-substrate pads adapted to support wire-bonding within a substrate as follows:

> However, Wang et al. ("Wang") discloses a semiconductor device that has intra-substrate pads adapted to support wire-bonding within a substrate (For Example: See Figure 2c). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include intra-substrate pads adapted to support wire-bonding within a substrate as disclosed in Wang because it aids in providing interconnection to other components (For Example: See Figure 2). That statement is incorrect, in view of wireless multi module technologies as of 3/18/2004 and general requirements for a wireless module with active and passive substrates with intra-substrate pads adapted to support wire-bonding within a substrate. One skilled in the art would NOT have made a combination with Kawai, Riches and Wang as of 3/18/2004 for the following reasons.

3. First, none of the references show the claimed intra-substrate bonding. The term "intra-substrate bonding" in the present application covers bonding(s) done completely within a semiconductor IC and is NOT about bondings made between different ICs (such as Kawai's bonding 6 between pads 15a and 5b positioned on different chips 2 and 10 mounted above a module base (such as Kawai's module base 20). For example, as shown in FIG. 1 of the instant application, intra-substrate bondings are shown for the amplifier IC 20 and the bonding pads are completely within the amplifier IC 20.

4. The Wang substrate is a multi-layer material built up as the module base to attach semiconductor ICs, and is NOT a semiconductor IC itself. Wang's Fig. 2c refers to pad definitions on the module base. These pads on Fig. 2c provide bonding on the same multi-layer material that forms the supporting base, NOT the intra-substrate bonding on the IC such as the intra-substrate bondings on the IC 20 of FIG. 1 of the instant application.

5. In the instant application, the intra-substrate pads and the wire-bonding among intra-substrate pads within a semiconductor IC such as the IC 20 are done to provide electromagnetic characteristics that are useful in certain radio frequency (RF) circuitry. For example, such intra-substrate wire-bonds can be used to vary resistance/capacitance/ inductance (RCL) characteristics useful for RF circuitry. Hence, the intra-substrate bonding on the IC is done to achieve a technical function that is different from the wiring for interconnection purposes of Kawai, Riches and Wang as asserted in the Final Office Action.

6. Second, the combination of Kawai, Riches, and Wang would result in an inoperable device. Riches disclose CMOS MCM substrates. Wang discloses flip chip assembly via reflowable underfill. However, Wang's flip chip assembly technique would not work with IC dies having rough surface morphology such as the GaAs HBT IC that is used as the active die 20 in FIG. 1 of the instant application. One skilled in the art would not combine the dies of Kawai and Riches with the Wang flip-chips because such a combination would not work.

7. Third, one skilled in the art would not have combined Kawaii, Riches and Wang to arrive at active and passive IC modules with intra-substrate pads adapted to support wire-bonding within an IC substrate. As noted at http://www.microbonding.com/gb/fc_gb.htm, "flip chip technology is cheaper than wire bonding (true also with TAB) because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time." In this case, one skilled in the art would not have done flip-chip and then wirebond two pads that are completely within an integrated circuit (IC) die. Combining the references as suggested by the Examiner would not be economical and one skilled in the art would not be motivated to combine as suggested as it is cheaper to provide interconnection using lines fabricated directly on the IC rather than to bond wires between pads on the IC.

8. In summary, neither Kawaii, Riches nor Wang provides a wireless module with active and passive substrates which are semiconductor ICs having intra-substrate pads adapted to support wire-bonding within these semiconductor ICs. As discussed above, none of the references show the claimed intra-substrate bonding on a semiconductor IC for design reasons. Kawaii, Riches and Wang disclose the use of multiple substrates for very different applications. Wang shows a multi-layer material used as a substrate for chip placement, but Wang does NOT show the intra-substrate bonding within a semiconductor IC.

Respectfully submitted,

Weiping Wang

Weiping Wang, Ph.D.